Optoelectronic Device Fabrication

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Optoelectronic devices are a core technology at LLNL. In order to fabricate many of the desired opto-electronic devices, plasma etching is frequently required to construct structures with 3-D shapes. Additionally, plasma etching is required to connect multiple devices within a semiconductor wafer. The plasma etching that is needed requires vertical and smooth sidewalls to allow for such integration and also for device performance.

In this project we have addressed the device integration requirements by determining methods to fabricate turning mirrors. We also have a large effort in the area of pillar fabrication, which is being considered for thermal neutron detectors. In this area we have made advances in terms of fill factor and aspect ratio, as well as the determination of process recipes to fabricate a demonstration device. This is a two-year project and the signal routing component was addressed in the first year of the project (FY2005), while the second year of the project is primarily concerned with the pillar fabrication methods and the required techniques to fabricate a demonstration device for thermal neutron detection.

Project Goals

For data routing we will create turning mirrors, splitters and combiners. The fabrication processes studied satisfy requirements of specific ongoing projects as well as increase our technology toolbox. Pillar structures are demonstrated with a geometry of at least 100 x 100 pillars with a fill factor of 50 %, (where the fill factor is the percent of semiconductor used for pillars). Additional microfabrication tasks will be carried out in order to demonstrate a pillar-structured neutron detector.

Relevance to LLNL Mission

This work is supporting both internally- and externally-funded projects that require advanced InP-, GaAs- and Si-based process technology. There are many different devices having broad applications that share the same fabrication hurdles. Having this technology will allow deployable microfabricated systems for several applications that are at the core of LLNL's national security missions, such as: high-speed radiation diagnostic devices for NIF, single-transient recording technologies, devices for encryption applications, and radiation detection.

FY2006 Accomplishments and Results

The work focusing on data routing elements for inverters was carried out in FY2005. The scope of work for FY2006 is focused on building a technology toolbox required to fabricate a pillar-structured neutron detector. Two major areas were enhanced: 1) high-aspect-ratio etching, and 2) fabrication methods for a demonstration detector (see figure).

Within the high-aspect-ratio etching work, we have increased our aspect ratio to 10. This yields 2-µm-diameter pillar geometry, with a 2-µm separation and 20-µm pillar etch depth. The fill factor for this pillar area is 50 % for our 1-cm-x-1-cm chip.

Within the area of demonstration detector fabrication, we implemented processing recipes for our pillar-structured neutron detector. This included the specification and procurement of lithographic masks, the evaluation of methods to deposit the boron materials, which is the neutron-converting material for this particular device, as well as lapping, polishing and etching techniques of boron. Processes to fabricate low-resistance contacts to silicon were demonstrated. This included ohmic contact formation to both p+ and n+ silicon: for p+ Si a platinum/titanium/gold multi-layer stack, (400/400/2000 Å), and for the n+ side, a titanium single layer (2000 Å). Both of these metallization schemes form a silicide upon annealing, yielding a low-resistance metal contact of $R_C < 10^{-5}\ \Omega\text{-cm}^2$.

Related References

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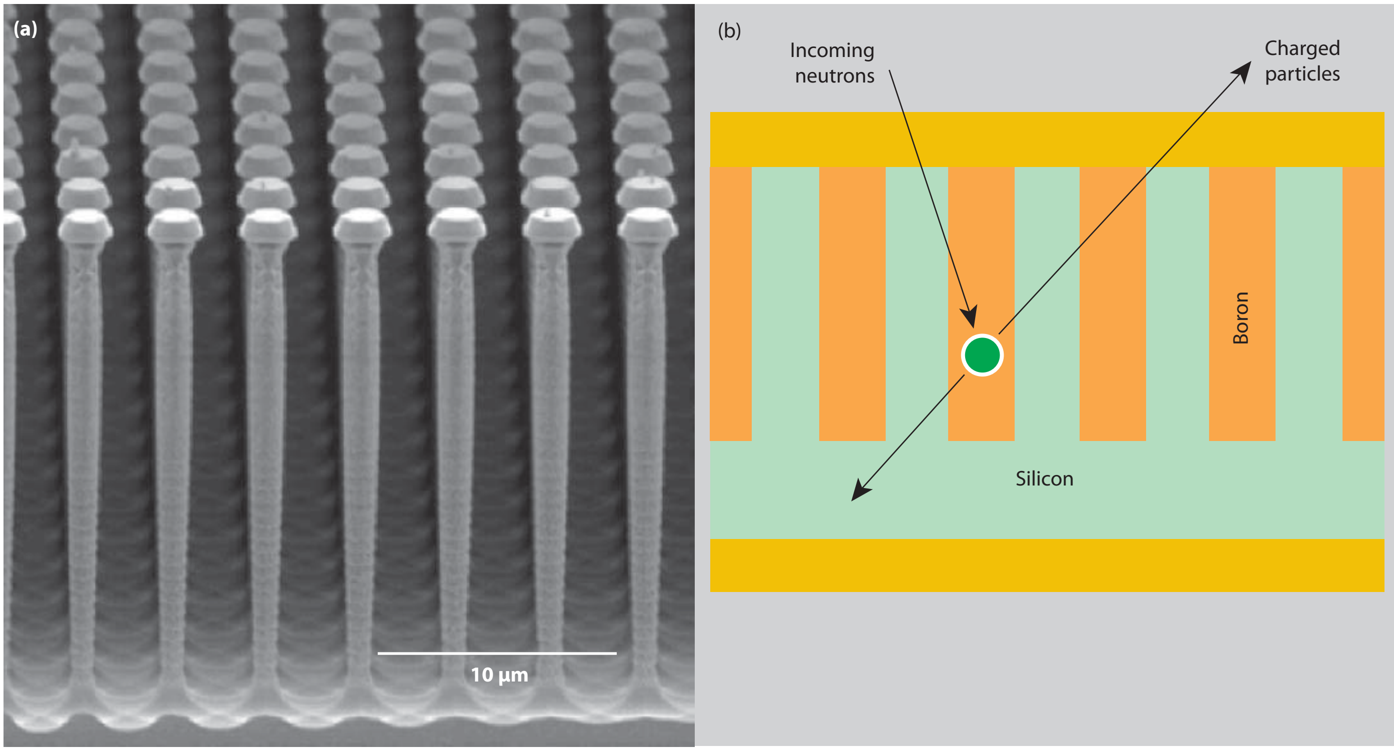

(a) Micrograph, showing the etched silicon pillars used in the Pillar Detector. Pillars are 20 µm in height and spaced about 2 µm apart. (b) Thermal neutron detector: incoming neutrons interact with the pillars within a semiconductor matrix.